Incomplete section 1 of user manual. See andahammer.com downloads page for the latest manuals.

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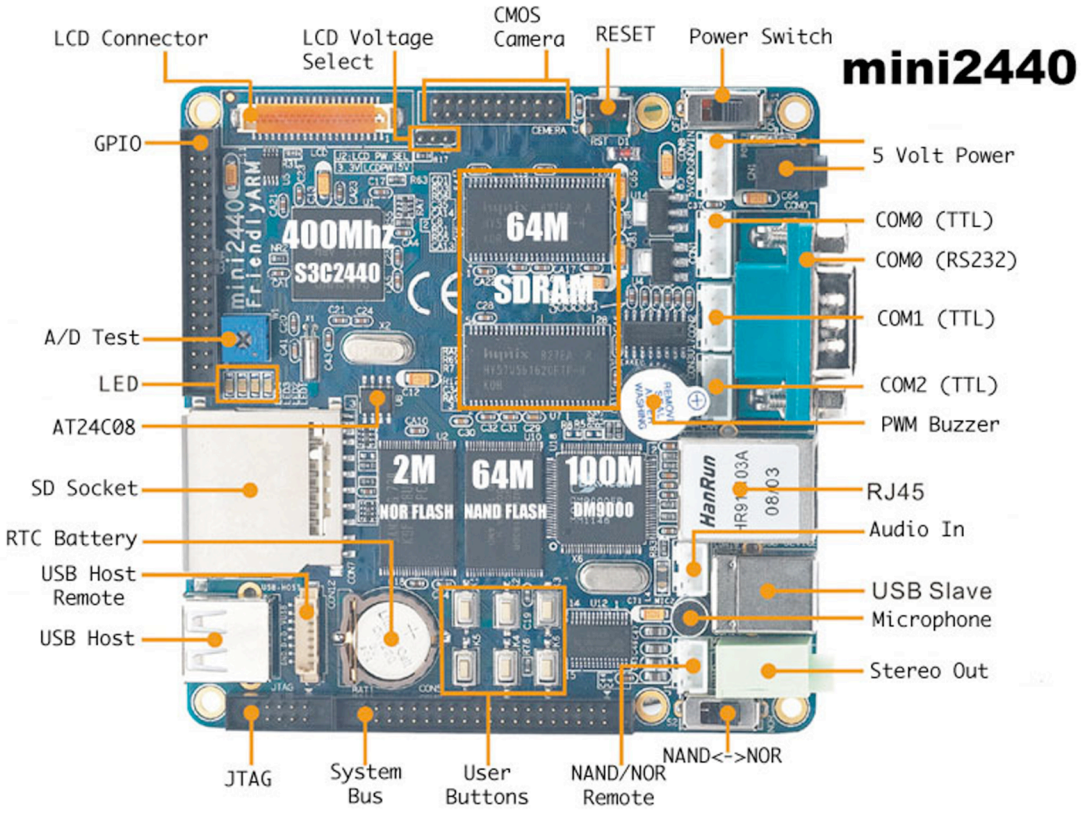
MINI2440 Introduction

About 1.1 MINI2440

The mini2440 is a practical low-cost ARM9 Single Board Computer (SBC) with a very high performance/cost ratio. With the Samsung S3C2440 microprocessor and the use of professional layout and quality peripheral chips, it is very robust. The Mini2440 uses a four-layer board with gold immersion processing, and has high quality equal-length bus routing in timing critical areas. The production environment and quality control are the same as those of modern high-speed motherboards.

1.1.1 MINI2440 Component Side



1.1.2 MINI2440 features and hardware resources

Processor - Samsung S3C2440A, 400MHz (Max 533Mhz)

RAM

- On-board 64M SDRAM
- 32bit data bus
- clock frequency up to 100MHz

FLASH storage

- 64MBytes Nand Flash
- 2MBytes Nor Flash with installed BIOS

LCD Interface

- 4-wire Resistive Touch Panel interface -- 10 bit A/D
- Supports 4 and 16 level gray-scale, 256 color, 4096 color STN LCD
- screen size from 3.5 inch to 12.1 inch
- screen resolution up to 1024x768
- Support 4 and 16 level gray-scale, 256 color, 64K color, True Color TFT LCD
- screen size from 3.5-inch to 12.1-inch
- screen resolution to 1024x768 pixels
- Configuration for the NEC 240x320/3.5-inch TFT true color LCD with Touch Panel

Interface and resources

- 1 10/100M Ethernet RJ-45 interface (DM9000 network chip)
- 3 serial ports - one configured for RS-232, COM0
- 1 USB Host
- 1 USB Slave B-type interface
- 1 SD card storage interface, no size limit
- 1 Channel Stereo audio output interface,
- 1 Built in microphone
- 1 Microphone input.
- 1 2.0mm pitch 10-pin JTAG interface
- 4 USER LEDs
- 6 USER buttons (with connection to GPIO connector and 8 pin user connector)
- 1 buzzer PWM control
- 1 adjustable resistor for A/D test
- 1 IIC bus AT24C08 chip for IIC Bus Test or configuration data, holds 256 bytes.
- 2.0 mm pitch 20PIN camera interface
- Power Interface (5V), with power switch and indicator light

System Clock Source

- Passive crystal
- Internal real-time clock (with back-up lithium battery)

Expansion Interface

- 1 34 pin 2.0mm GPIO interface

1 40 pin 2.0mm system bus interface

Size

100 x 100 (mm)

Supported Operating Systems

Linux 2.6.29

WindowsCE.NET 5.0/6.0

uC/OS-II

1.1.3 CD-ROM resources

(1) ADS1.2 Setup

(2) H-JTAG debugging software programmer

(3) Windows Flash programmer software SJF2440

(4) Linux Nand Flash programmer software Jflash-2440 (with source code)

(5) Serial tools CRT, dnw

(6) C language tool chain

(7) USB drive (WindowXP/2000 under installation)

(8) vivi source code for Linux. (The bootloader.)

(9) Test code for LED lights on the board.

(10) A collection of sample apps that test system I/O.

(11) WindowsCE BSP and sample project files

(12) linux development tools and kernel source code package:

- Arm-linux-gcc-4.3.2 tool chain used for kernel, Qtopia 2.2.0, user apps.
- Yaffs file system mapping tool mkyaffsimage
- Linux-2.6.29 for MINI2440 kernel source code (including the DM9000 driver, all kinds of TFT LCD drivers, sound card driver, Touch Panel Driver, YAFFS source code, SD card driver, RTC driver, serial port expansion drive, the USB camera driver, USB mouse and keyboard, USB drives, etc.)

(13) Embedded graphical interface.

Qtopia source code package.

Embedded browser source code package.

(14) Mini2440 schematic diagram (PDF format).

(15) User's manual (pdf format)

1.2 Interface layout and jumpers.

1.2.1 Jumper Description.

There is only one on-board jumper, J2. It is used to select the LCD driver board input voltage. For NEC3.5-inch LCD, set voltage selector for 5V.

1.2.2 Interface Layout

Mini2440 interface layout is shown in the diagram above. An optional cable and connector kit has a cable for every connector and a connector for every cable.

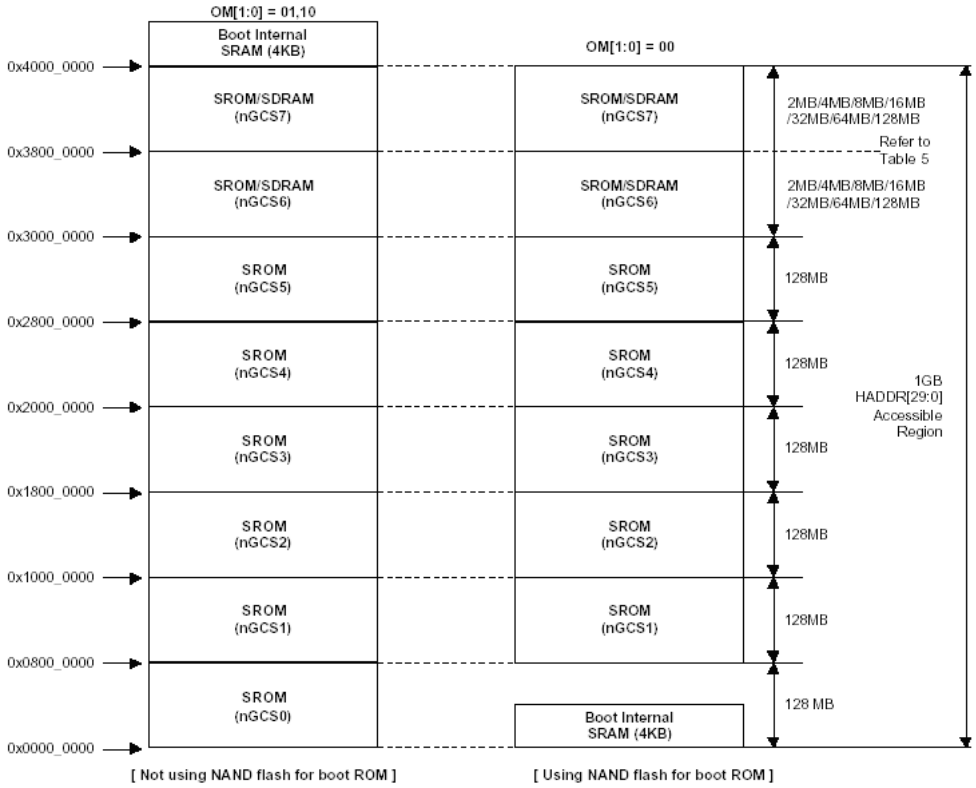
1.3 Interface resources.

This section details each interface or module with pin definitions and occupied CPU resources.

1.3.1 address space allocation and the definition of chip select signals.

The S3C2440 supports two modes: Boot from NAND Flash or boot from NOR Flash.

The boot mode determines the configuration of the memory map as shown in this table.



When the NOR/NAND switch is in the NOR position, the system conforms to the memory map on the left. In the NAND position, the The S3C2440 uses the memory map on the right.

SFR Area for special control register addresses:

The following are the device address space allocations and the definition of the chip select signals. The nGCS0 chip select space is different depending onstart-up mode. In NAND Flash boot mode the internal 4K Bytes - BootSram - is mapped to nGCS0 Space.

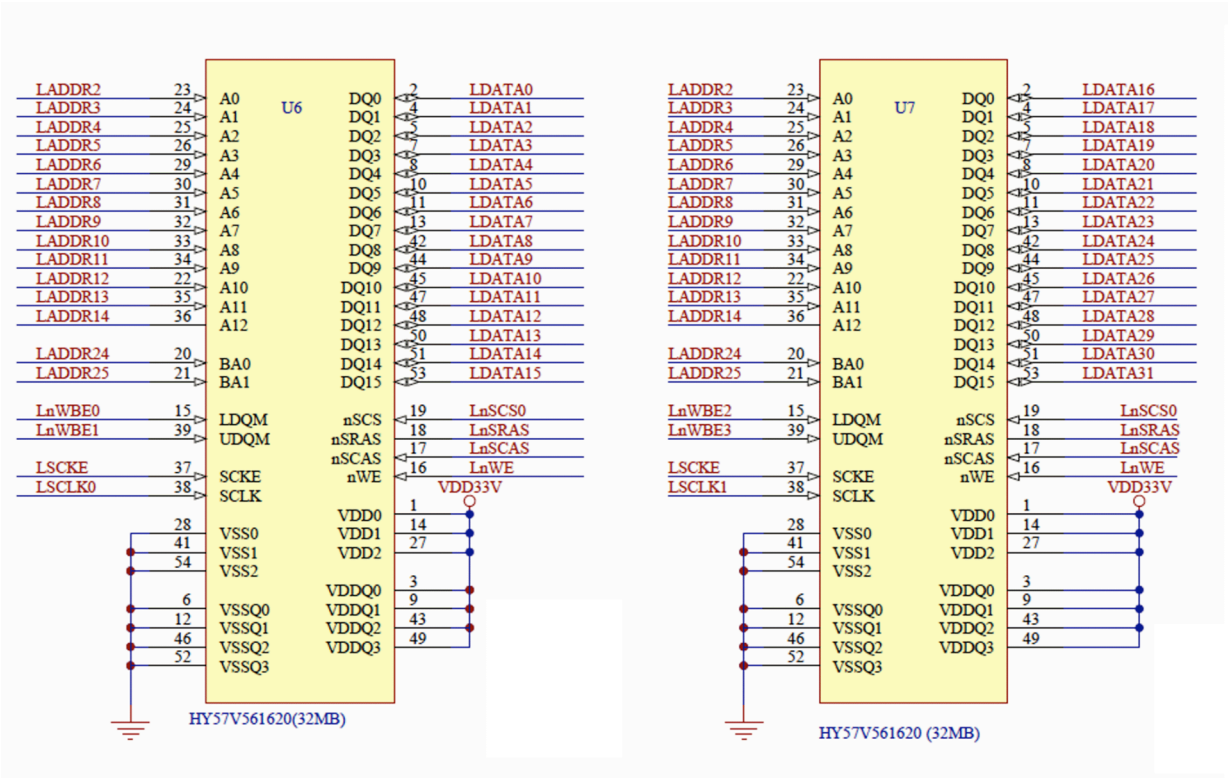
In Nor Flash start mode (non-Nand Flash Boot Mode), nGSC0 is connected to external memory. Nor Flash has been mapped to the chip select space nGCS0

The 64 MByte SDRAM address space is: 0x30000000 to 0x34000000

1.3.2 SDRAM storage systems

The Mini2440 uses two external 32MByte SDRAMs for a total of 64M bytes of SDRAM memory which together form a 100 MHz 32-bit data bus RAM. With its 16K each of data and instruction cache running at over 400 MHz, the whole system performs much as if it had 400 MHz external buses.

Here is the SDRAM portion of the schematic.

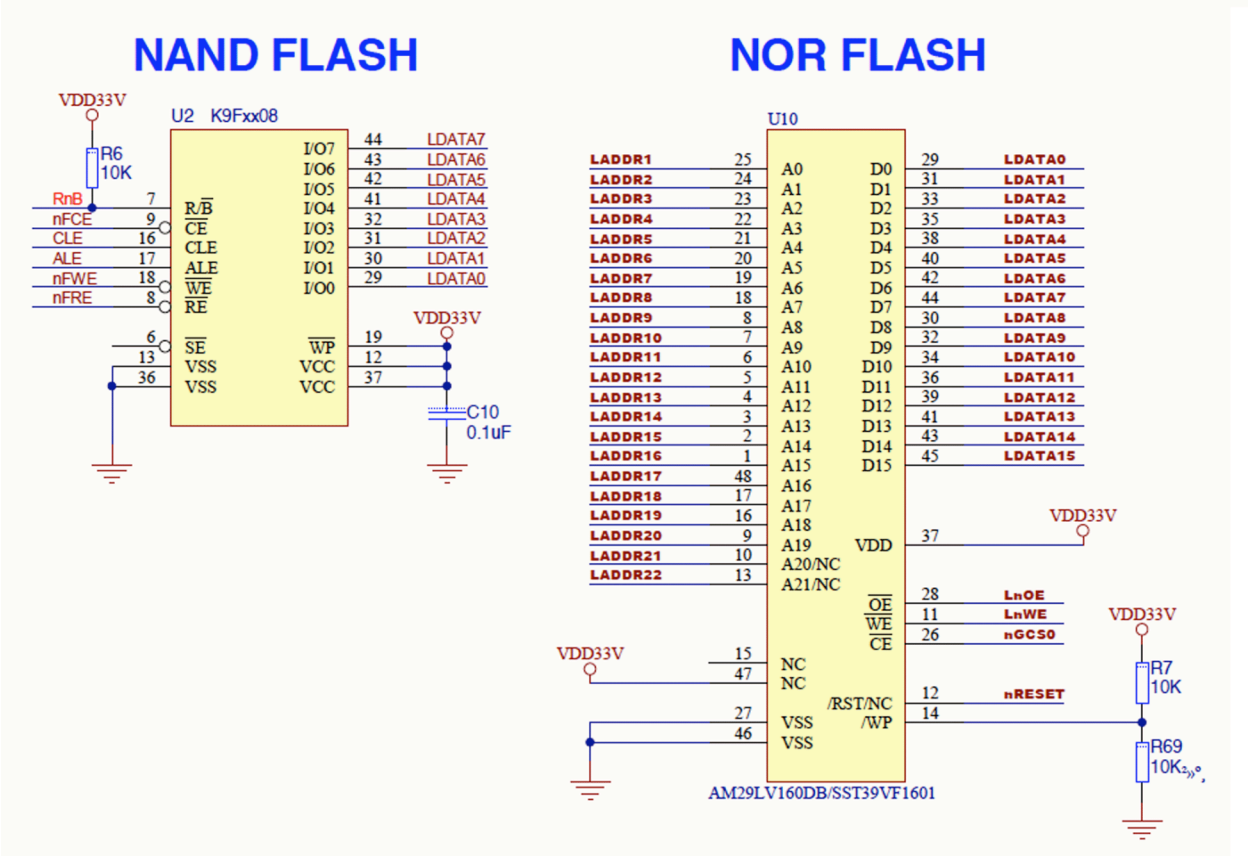


1.3.3 FLASH storage systems

The Mini2440 has two kinds of Flash, one is the 2MByte Nor Flash, model SST39VF1601. The other is the 64 MByte Nand Flash model K9F1208. The S3C2440 supports starting from either Flash. The slide switch, S2, chooses Nand or Nor. The Nor Flash uses A1-A22 for a total of 22 address lines. Why not A0? Because the memory is 1 word or two bytes (16 bits) wide and all access is on even numbered addresses. The smallest unit read is two bytes.

According to the schematic, the design could use a total of 8 Mbyte of Nor Flash. On the SST39V1601 chips, A20 and A21 have no connection, allowing 2 Mbytes of Nor flash.

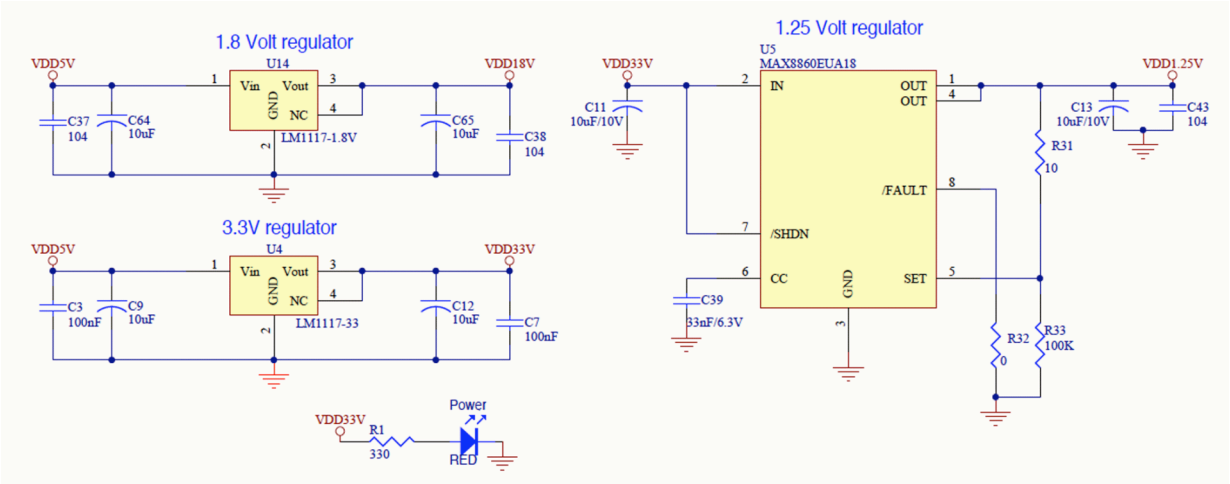
The 64 MByte Nand Flash is only 8 bits wide. Again, the 16k data and instruction caches allow reasonable speed even if running code from Nand memory. (Most code is made of loops and sections that repeat. Once in cache, they run at full 400 MHz speed. The Harvard architecture of the ARM9 allows fetching and pipelining instructions and data simultaneously from the two caches, giving exceptional performance.)



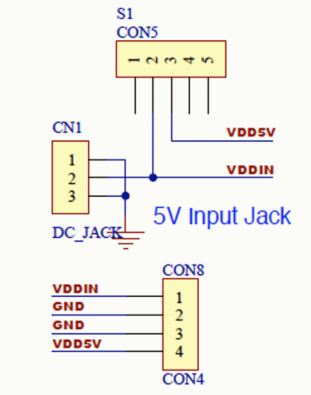
1.3.4 Power Supplies

The Mini2440's power supply system is rather simple and requires an external 5V power supply. Three regulators are used to generate 3.3V, 1.8V, and 1.25V.

Please note: The Mini2440 is not designed for handheld mobile devices, so it does not have full power management circuitry. The S1 DIP switch controls the system power and there is no provision for power control through software.

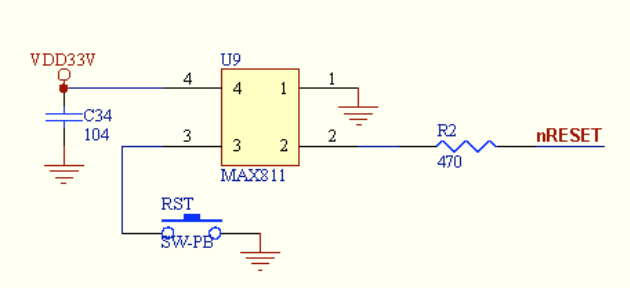


Most installations eventually need a power connection more permanent than a simple barrel jack. CON8 should be used to supply the 5V power. This 2.0mm pitch single row socket needs 5V on each outside pin and both inner pins are GND. Note that the two input voltages are not connected. VDDIN powers the on-board parts through the regulators. VDD5V goes to CON5, the system bus expansion connector.



1.3.5 System Reset

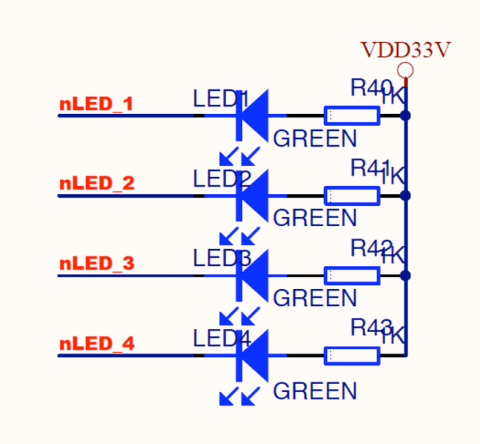
The Mini2440 conditions reset with the MAX811 reset chip to provide a clean low level reset to the CPU.



1.3.6 User LED

LEDs are commonly used for status indication. The Mini2440 has four user-programmable LEDs. They are connected to the S3C2440 GPIO lines and are active-low (light on when signal is low).

LED1	LED2	LED3	LED4
GPB5	GPB6	GPB7	GPB8



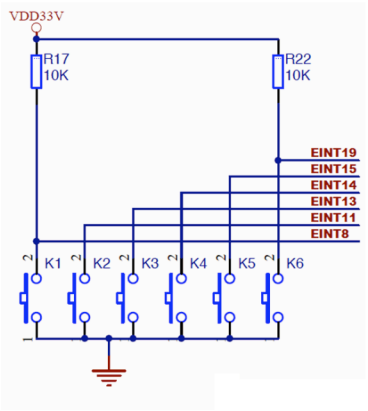
1.3.7 User buttons or keys.

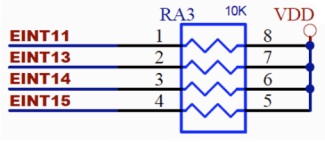
The user buttons are controlled by Port G, which can be used to assign several functions to the pins. The Mini2440 has a total of 6 user test buttons connected directly to the CPU interrupt pins. The active-low signals are held high by 10K resistors R17 - R22. Connector 12 has the same 6 user button signals with ground and VDD (3.3V). No external pull-up is needed. Pins 1 - 6 on Connector 12 are defined as K1 through K6 to match the on-board buttons. You can use more than one switch on each line.

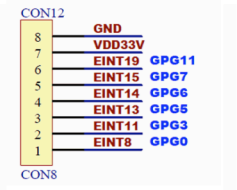
The 6 user buttons correspond to external interrupts EINT8 EINT11 EINT13 EINT14 EINT15 EINT19 and depending on resister settings, can also be set to GPIO GPG0 GPG3 GPG5 GPG6 GPG7 GPG11 or nSS1 SPIMISO1 SPIMOSI1 SPICLK1 TCLK1

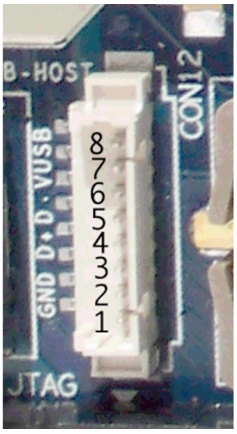
The Connector-12 functions are determined by Port G. See the S3C2440 Data Sheet for Port G details.

Port G Control Register →	10xx 101010xx 10xxxx10	11xx 111111xx 11xxxx11	00xx 000000xx 00xxxx00 in 01xx 010101xx 01xxxx01 out
Con12.1	EINT8		GPG0
Con12.2	EINT11	nSS1	GPG3
Con12.3	EINT13	SPI MISO1	GPG5
Con12.4	EINT14	SPI MOSI1	GPG6
Con12.5	EINT15	SPI CLK1	GPG7
Con12.6	EINT19	TCLK1	GPG11
Con12.7	Vdd 3.3V		
Con12.8	GND		



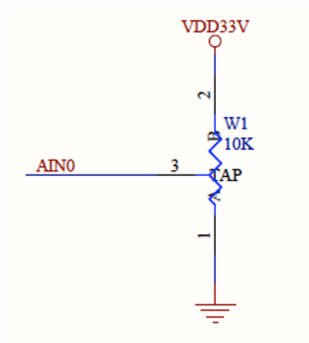






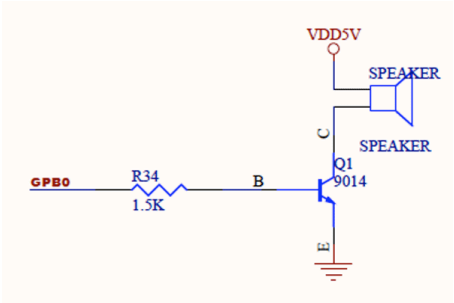
1.3.8 A/D input test.

The Mini2440 has an 8-channel 10 bit A/D converter with sample and hold. When a touchpad is used, 4 channels are dedicated to touch pad conversion. The other 4 are general purpose and are on connector 4, GPIO. Pins 5, 6, 7, 8 are AIN0, AIN1, AIN2, AIN3. AIN0 is connected to a pot on the PCB for testing. If you need AIN0, remove the pot or cut the trace from the pot center pin to pin5 of CON4. The trace is on the bottom of the PCB with quite a bit of free space around it.



1.3.9 PWM Control buzzer

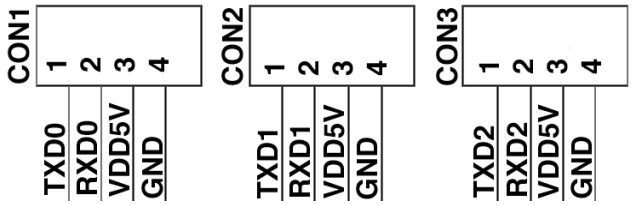
The Mini2440 has a small buzzer, which can be controlled (somewhat) through PWM. The signal is from GPIO pin 31 (GPB0).



1.3.10 Serial

The Samsung S3C2440 chip supports three serial ports UART0, UART1, UART2. Each has a connector with TTL level signals and also connects to CON4, the GPIO connector. UART0 also has TTL to RS-232 conversion and uses the COM0 DB9 connector to work with any RS232 device.

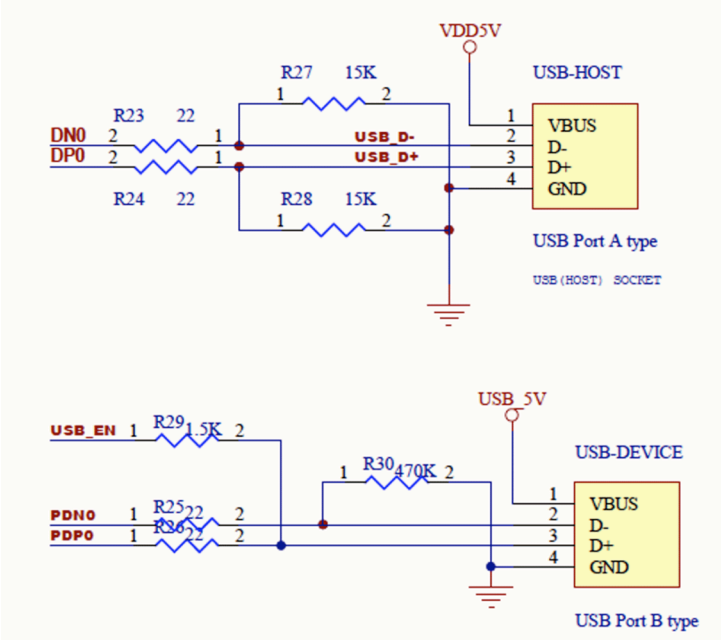
COM0 boots at 115,000 BAUD, N 0 1 and is fully supported by Linux and WinCE.



1.3.11 USB interface

The Mini2440 has two USB interfaces. A USB Host, like an ordinary PC's USB interface, can be used with a USB camera, keyboard, mouse, wifi dongle, etc. The USB Slave is the smaller squarish connector (like you find on printers) and is generally used to download to the target board. When the Mini2440 is running WinCE, it can ActiveSync software with Windows. When the Mini2440 is running a Linux system, there is no corresponding driver and application. Ethernet is usually preferred for data transfer in Linux.

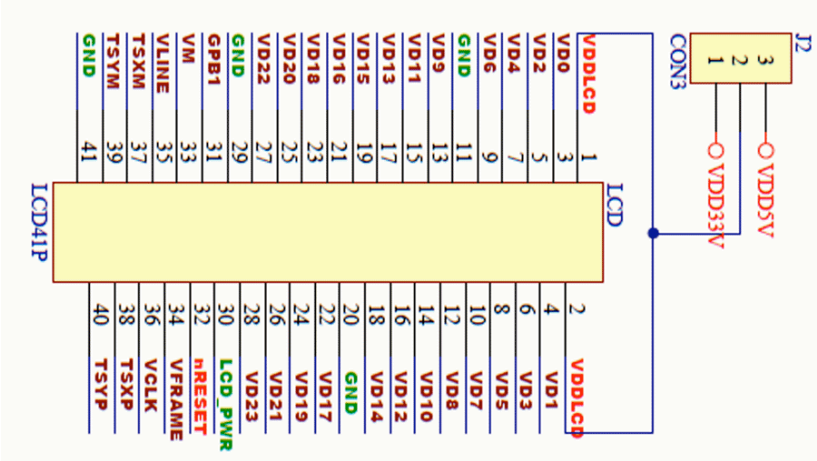
The USB Slave can be controlled with a GPC5 register bit to set USB_EN or disable. It can be disabled to conserve CPU resources.



1.3.12 LCD interface

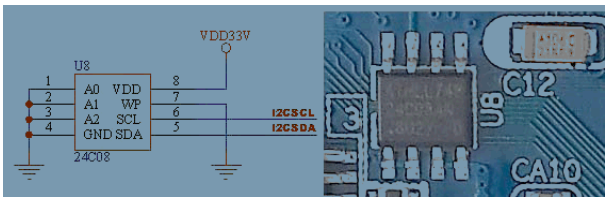
The Mini2440 LCD interface has a 41 Pin 0.5mm pitch white connector, which contains common LCD control signals (line-field scanning, the clock, enable, etc.) and complete RGB output of 8:8:8, supporting a maximum of 16 million colors. The LED backlight can be turned on or off with GPB1. The backlight signal is called LCD_PWR PWM output and reset signals (nRESET), one of the backlight control signals is LCD_PWR.

In addition, pins 37, 38, 39, 40 are for the four-wire touch screen interface. They can be directly connected to a Touch Panel. See figure J2 for the LCD driver board power supply select signal. All the currently used LCD controllers use a 5V power supply.



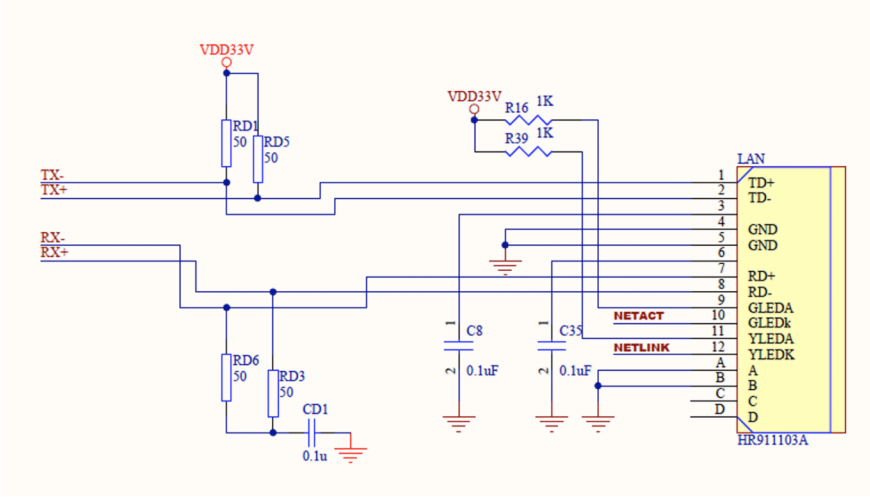
1.3.13 EEPROM

The Mini2440 has a direct connection from the S3C2440 I^2C signal pin to an AT24C08 EEPROM with a capacity of 256 byte. This is mainly used to test the I^2C bus and I^2C code.



1.3.14 Network Interface

The Mini2440 uses a DM9000 10/100M LAN chip with network transformers and an RJ-45 connector. Ordinary Cat5e cable can connect from the Mini2440 to your routers or switches. Note: Each Mini2440's network MAC address is the same and can be configured by software. See section 2.4 for Linux. WinCE users refer to the BSP for the DM9000 driver code and the registry file (platform.reg).



1.3.15 Audio Interface

The S3C2440's built in I2S bus interface is directly connected to an external 8/16 bit stereo CODEC. The Mini2440 to adopt

Based on the I^2S bus UDA1341 audio decoder chip implementation system, the chip initializes internal registers and settings are taken

L3-bus with bus connection control of the implementation, where we have used a Samsung design of public board, respectively, using the CPU's GPB2,

GPB3, GPB4 port analog implementation of the L3-Bus specification L3MODE, L3DATA, L3CLOCK, their initialization

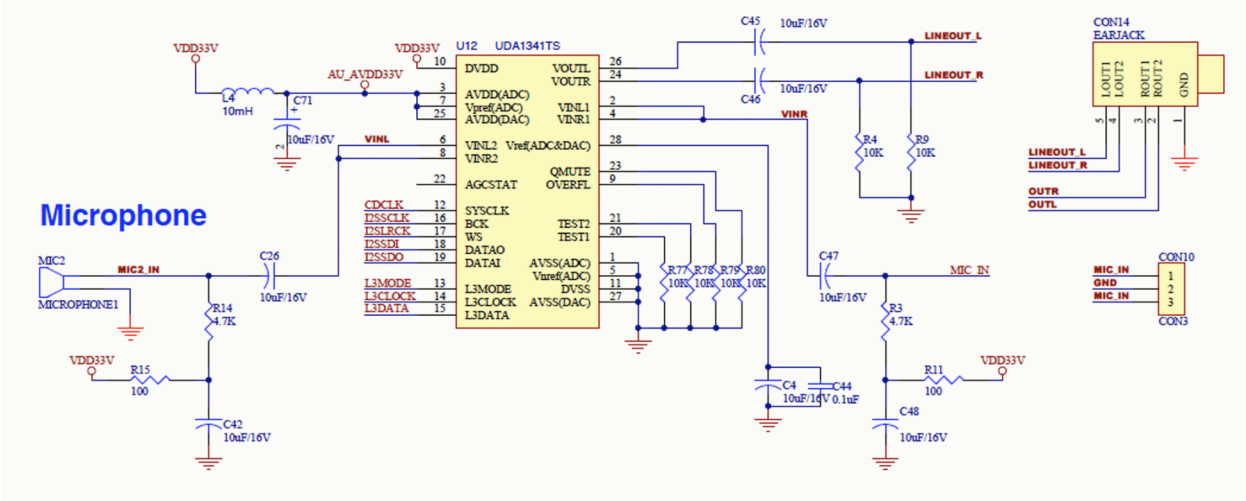
End after UDA1341 are no longer useful, so these three line of control can also use an ordinary single-chip analog implementation.

The output of audio systems for the development of on-board common aperture 3.5mm socket, input is divided into two roads, all the way for the onboard MAK

Grams of the wind, and the other road through the 2.0mm socket CON10 white leads. Two-way audio input of the driver are different, at present only

CON10 interface corresponding recording channel can be used, please refer to our website update information, the two channels of our most

Will drive up the end.



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